ABSTRACT

An interface circuit (1) for facilitating communication between an integrated circuit (2) and an external device (not shown) in either SPI protocol or one or both of I^2C and SMBus protocols, comprises a signal processing circuit (7), which is configurable in I^2C/SMBus and SPI protocol modes, and four communication terminals, namely, a CLK pin (3), and ADD/DOUT pin (4), and SDA/DIN pin (5) and a $\overline{CE}$ pin (6). On power-up of the interface circuit (1) the signal processing circuit (7) is configured in I^2C/SMBus protocol mode by a first mode select signal (V_{dd}) applied to a mode select input port (10) by a multiplexer (15) in response to a logic low switch signal from a switch signal flip-flop (22). A first state machine (20) outputs a logic low signal to an AND gate (21) for so long as the $\overline{CE}$ pin (6) remains continuously high or low, thus holding a reset input of the switch signal flip-flop (22) low. The first state machine (20) outputs a logic high in response to a protocol select signal on the $\overline{CE}$ pin (6), thus causing the reset input to go high, and in turn causing the switch signal flip-flop (22) to output a logic high switch signal, which operates the multiplexer (15) for switching a second mode select signal, namely, ground to the mode select input port (10) for configuring the signal processing circuit (7) in the SPI protocol mode. A locking circuit (23) holds the reset input of the switch signal flip-flop (22) low, thus maintaining the switch signal from the switch signal flip-flop (22) in the logic high state until the interface circuit is powered-down. Communication is carried out in SPI protocol using all four communication pins (3,4,5,6) and in I^2C/SMBus protocol using only the CLK pin (3) and the SDA/DIN pin (5).